PRELIMINARY DATA SHEET

SKY13484: 0.6-2.7 GHz DP12T (SP7T/SP5T) Receive Diversity Switch with MIPI RFFE Interface for Carrier Aggregation

Applications

- Carrier aggregation receive diversity systems (low band/high band)
- Embedded data cards

Features

- Low insertion loss, optimized for low and high bands
- Excellent Band 13 2nd harmonic performance (<–81 dBm)
- Excellent Band 17 3rd harmonic performance (<–100 dBm)
- Dual antenna ports can be connected externally to a low band/high band diplexer
- Integrated, programmable MIPI interface using separate registers for low and high bands
- Small MCM (22-pin, 2.5 x 2.9 x 0.8 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

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Description

The SKY13484 is a Single Pole, Five Throw (SP5T) and Single-Pole, Seven Throw (SP7T) Mobile Industry Processor Interface (MIPI) controlled antenna switch designed specifically for receive diversity in carrier aggregation applications.

The SP5T switch is optimized for the low band and the SP7T switch is optimized for the high band. Using advanced switching technologies, the SKY13484 maintains low insertion loss and high isolation for all switching paths. The high linearity performance and low insertion loss achieved by the SKY13484 makes it an ideal choice for carrier aggregation applications. The switch also exhibits excellent 2nd/3rd Order Intermodulation Distortion (IMD2/IMD3) performance.

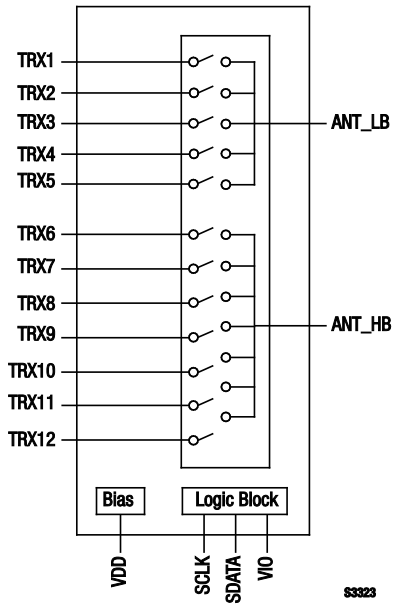

Figure 1. SKY13484 Block Diagram

Switching is controlled by an integrated MIPI decoder. The two switches can be configured independently. There are separate registers for low and high bands. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied to those paths.

The SKY13484 is manufactured in a compact, 2.5 x 2.9 x 0.8 mm, 22-pin surface mount Multi-Chip Module (MCM) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

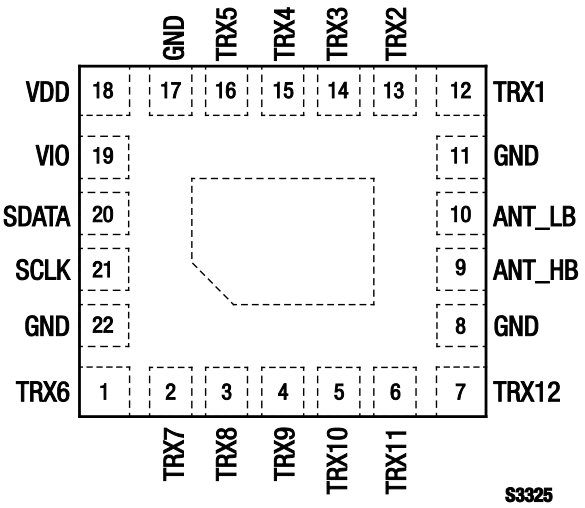

Figure 2. SKY13484 Pinout – 22-Pin MCM (Top View)

Table 1. SKY13484 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	TRX6	High band transmit/receive port 6	12	TRX1	Low band transmit/receive port 1
2	TRX7	High band transmit/receive port 7	13	TRX2	Low band transmit/receive port 2
3	TRX8	High band transmit/receive port 8	14	TRX3	Low band transmit/receive port 3
4	TRX9	High band transmit/receive port 9	15	TRX4	Low band transmit/receive port 4
5	TRX10	High band transmit/receive port 10	16	TRX5	Low band transmit/receive port 5
6	TRX11	High band transmit/receive port 11	17	GND	Ground
7	TRX12	High band transmit/receive port 12	18	VDD	DC power supply
8	GND	Ground	19	VIO	Interface supply voltage
9	ANT_HB	High band antenna port	20	SDATA	Data
10	ANT_LB	Low band antenna port	21	SCLK	Clock
11	GND	Ground	22	GND	Ground

Note: Bottom ground paddles must be connected to ground.

Table 2. SKY13484 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}		6	V
Digital control signal	VIO		2	V
SCLK port voltage	SCLK		VIO	V
SDATA port voltage	SDATA		VIO	V
RF input power	P_{IN}		+31	dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–30	+90	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13484 are provided in Table 2. Electrical specifications are provided in Tables 3 and 4.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 5 and 6, respectively.

Triple Beat Ratio frequencies are listed in Table 7.

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX12 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13484 exhibits exceptional performance for all TRXx ports.

Table 8 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figure 4 provides the timing diagram for register write commands.

Register descriptions and programming information is provided in Table 9.

Tables 10 and 11 provide the Register_0 and Register_1 logic, respectively.

Table 3. SKY13484 RF Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.6		2.7	GHz
Insertion loss	IL	TRX1 to TRX5, low band:				
		704 MHz		0.40	0.50	dB
		824 to 960 MHz		0.45	0.55	dB
		TRX6 to TRX12, high band:				
		1710 to 2170 MHz		0.6	0.65	dB
		2170 to 2690 MHz		0.7	0.80	dB
Isolation	Iso	ANT_LB to any “off” TRXx low band port:				
		Up to 704 MHz	28	30		dB
		Up to 960 MHz	26	28		dB
Isolation	Iso	ANT_HB to any “off” TRXx high band port:				
		Up to 1990 MHz	26	28		dB
		Up to 2170 MHz	24	26		dB
		Up to 2690 MHz	22	25		dB
Isolation	Iso	Any low band port (TRX1 to TRX5) to any high band port (TRX6 to TRX12) up to 960 MHz	25	30		dB
“On” state match	VSWR	Up to 2.7 GHz			1.5:1	–
2nd Order Intermodulation Distortion	IMD2	See Table 5	–105	–110		dBm
3rd Order Intermodulation Distortion	IMD3	See Table 6	–105	–110		dBm
Triple Beat Ratio (650 to 900 MHz)	TBR	See Table 7	+51	+81		dBc
Low band 2nd and 3rd harmonic	2fo, 3fo	TRX1 to TRX5, P_{IN} = +24 dBm, f = 900 MHz		–65		dBm
Low band 2nd and 3rd harmonic	2fo, 3fo	TRX1 to TRX5, P_{IN} = +24 dBm, f0 = 900 MHz, VSWR = 5:1		–55		dBm
Band 13 2nd harmonic	2fo	TRX1 to TRX5, P_{IN} = +15 dBm, f0 = 782 MHz		–81		dBm
Band 17 3rd harmonic	3fo	TRX1 to TRX5, P_{IN} = +15 dBm, f = 707 MHz		–105	–100	dBm
Turn-on time	t_{ON}	From application of V_{DD} and VIO			20	µs
Wake up time	t_W	From isolation state		2	5	µs
Switching speed	t_S	Any state to any other state		2	5	µs

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 4. SKY13484 DC Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, VIO = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	6.00	V
Supply current, active mode	I_{DD}			50	100	µA
Interface supply voltage level	VIO		1.65	1.80	1.95	V
Interface signal: High Low	SDATA		0.7 × VIO		 0.3 × VIO	 V V
Control current: High Low					 10 5	 µA µA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 6. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 7. Triple Beat Ratio Frequencies and Power Levels

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker ANT (MHz)	Power Blocker (dBm)	Triple Beat Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ± 1
5	836.5	+21.5	881.5	+21.5	881.5	–30	881.5 ± 1

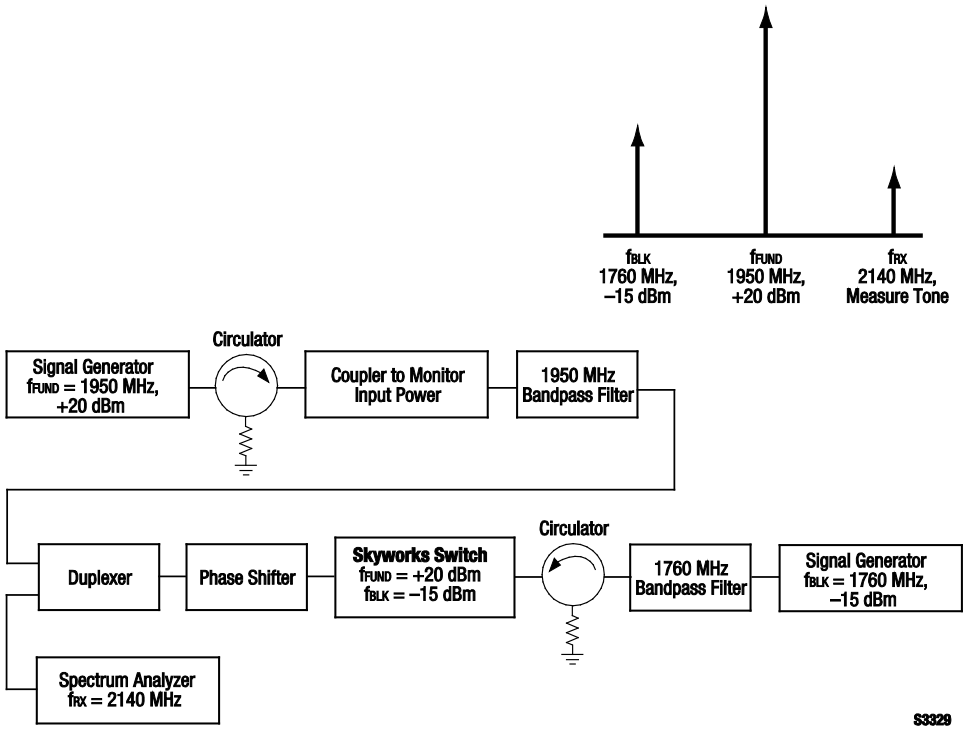

Figure 3. Typical 3rd Order Intermodulation Test Setup

Table 8. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg_0 Write, Short Command	Y	SA[3:0]	1b	Data[6:5]	Data[4]	Data[3:0]	Y	Y	–	–	–	–	–	–
Reg_0 Write, Long Command	Y	SA[3:0]	0	10b	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg_1 Write	Y	SA[3:0]	0	10b	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11b	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

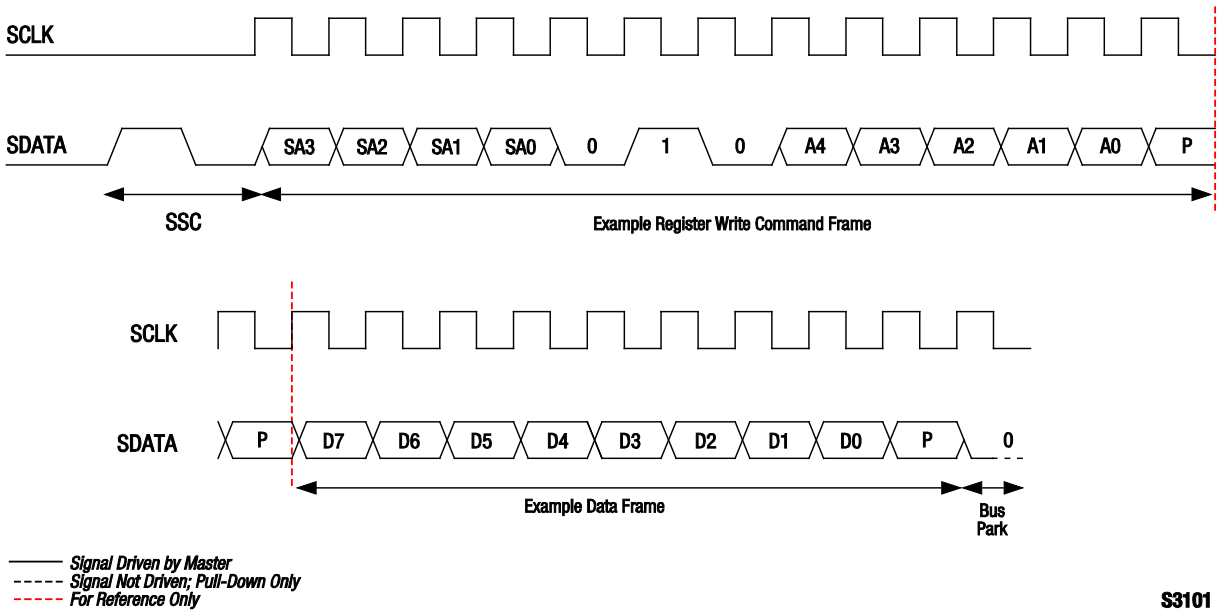

Figure 4. Register Write Command Timing Diagram

Table 9. Register Description and Programming (1 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[6:0]: See Table 10 for logic	0000000
Register_1	0001	MODE_CTRL	Bits[7:0]: See Table 11 for logic	00000000
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	01
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers (unsupported).	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01010000

Table 9. Register Description and Programming (2 of 2)

Register		Parameter	Description	Default (Binary)
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read-only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read-only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Table 10. Register_0 Truth Table (High Band)

State	Mode	Register 0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation (default)	x	x	x	x	x	0	0	0
2	TRX6	x	x	x	x	x	0	0	1
3	TRX7	x	x	x	x	x	0	1	0
4	TRX8	x	x	x	x	x	0	1	1
5	TRX9	x	x	x	x	x	1	0	0
6	TRX10	x	x	x	x	x	1	0	1
7	TRX11	x	x	x	x	x	1	1	0
8	TRX12	x	x	x	x	x	1	1	1

Table 11. Register_1 Truth Table (Low Band)

State	Mode	Register 1 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation (default)	x	x	x	x	x	0	0	0
2	TRX1	x	x	x	x	x	0	0	1
3	TRX2	x	x	x	x	x	0	1	0
4	TRX3	x	x	x	x	x	0	1	1
5	TRX4	x	x	x	x	x	1	0	0
6	TRX5	x	x	x	x	x	1	0	1

Evaluation Board Description

The SKY13484 Evaluation Board is used to test the performance of the SKY13484 DP12T (SP7T/SP5T) Switch. An Evaluation Board schematic diagram is provided in Figure 5. An assembly drawing for the Evaluation Board is shown in Figure 6.

Package Dimensions

The PCB layout footprint for the SKY13484 is provided in Figure 7. Typical case markings are shown in Figure 8. Package dimensions for the 22-pin MCM are shown in Figure 9, and tape and reel dimensions are provided in Figure 10.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13484 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

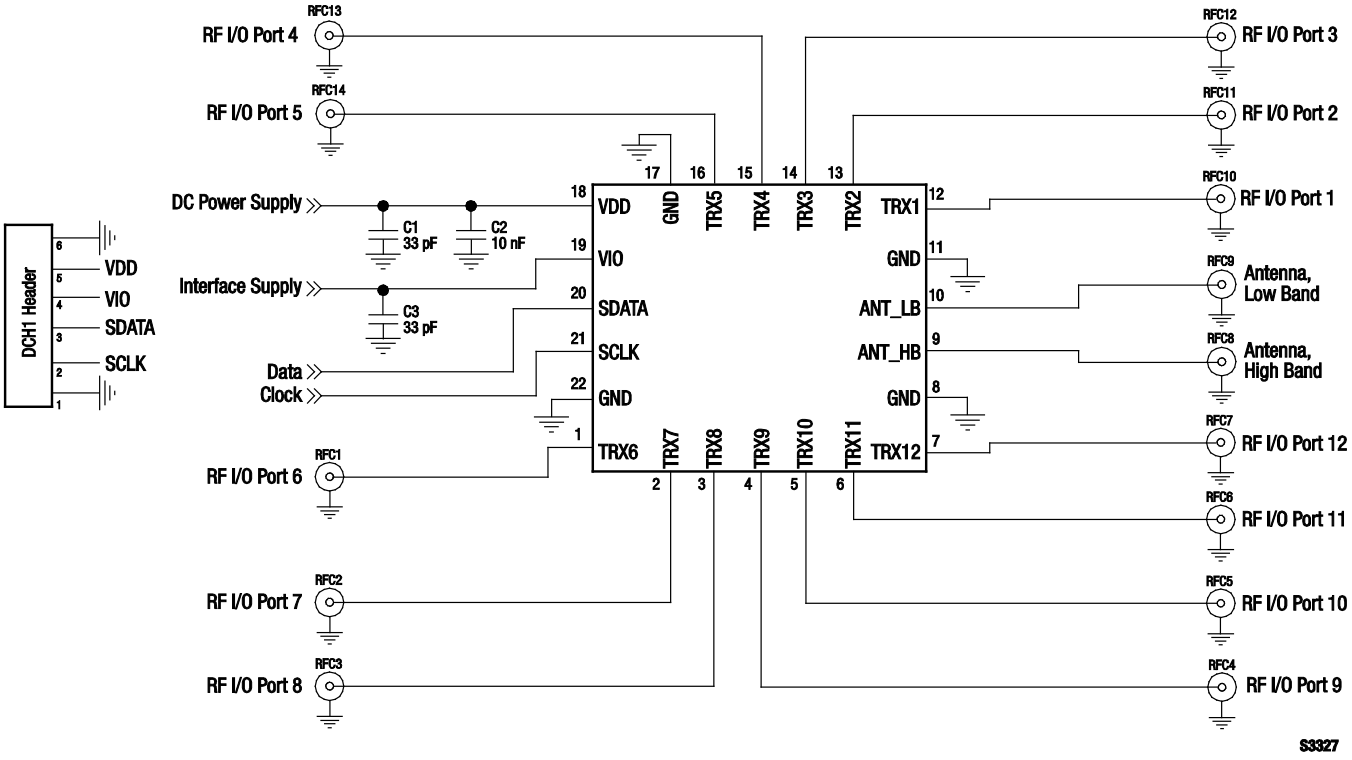

Figure 5. SKY13484 Evaluation Board Schematic

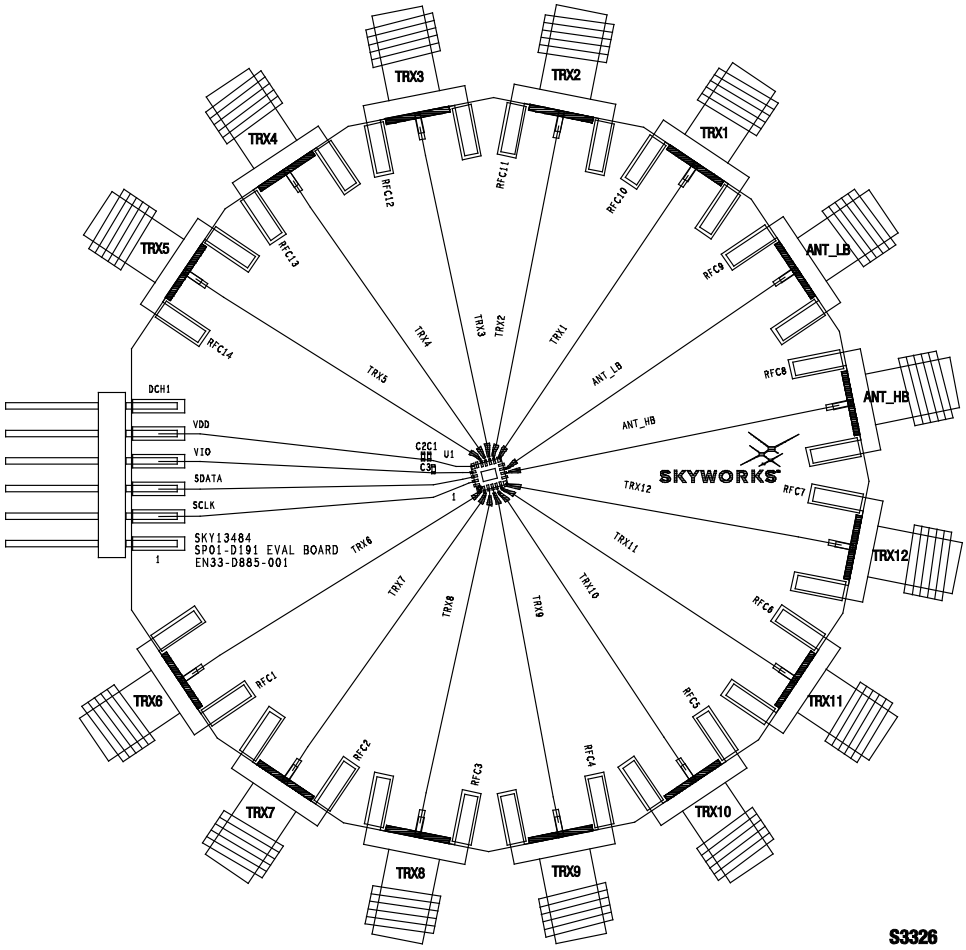

Figure 6. SKY13484 Evaluation Board Assembly Diagram

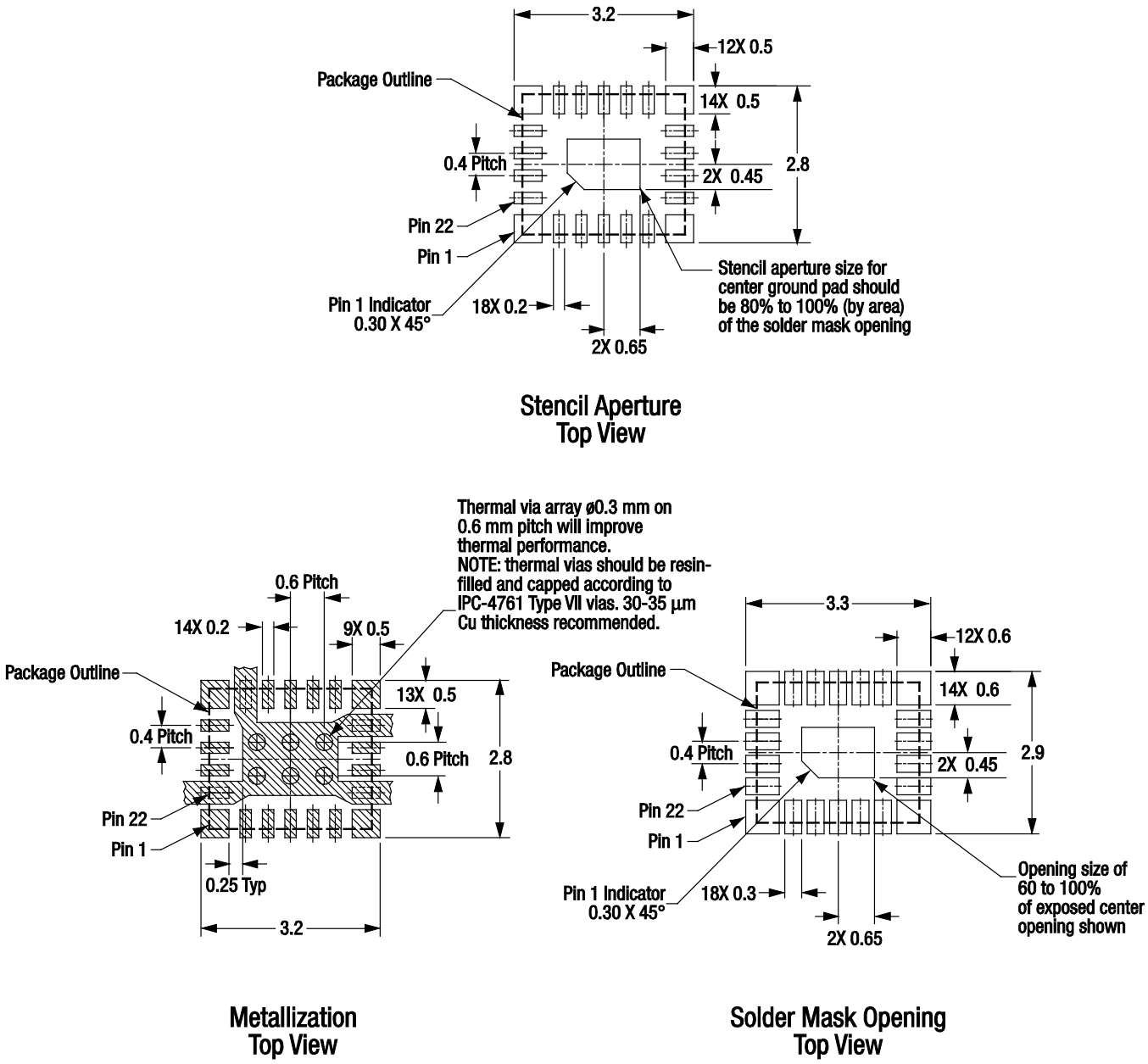

Figure 7. SKY13484 PCB Layout Footprint

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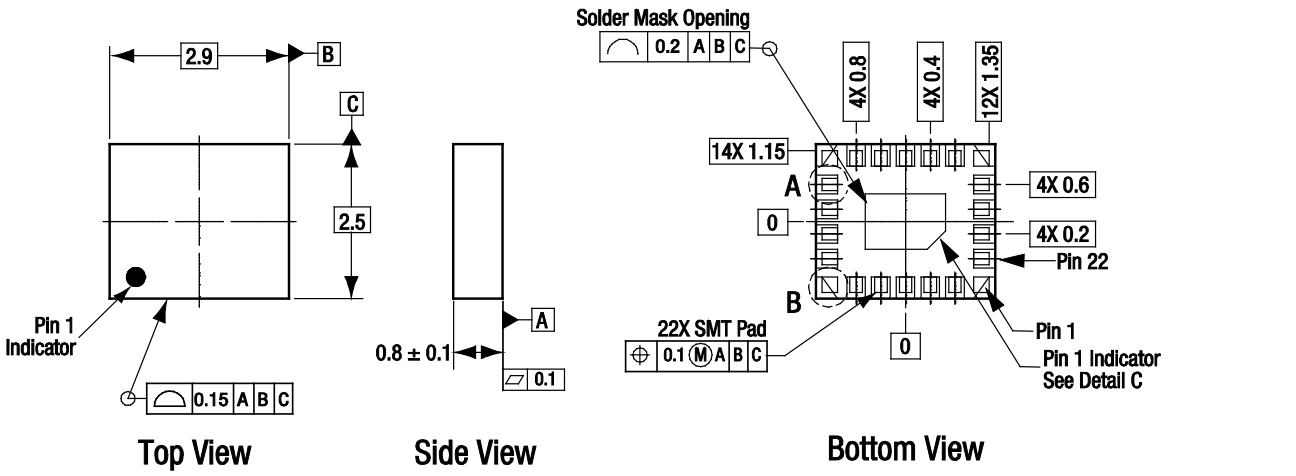
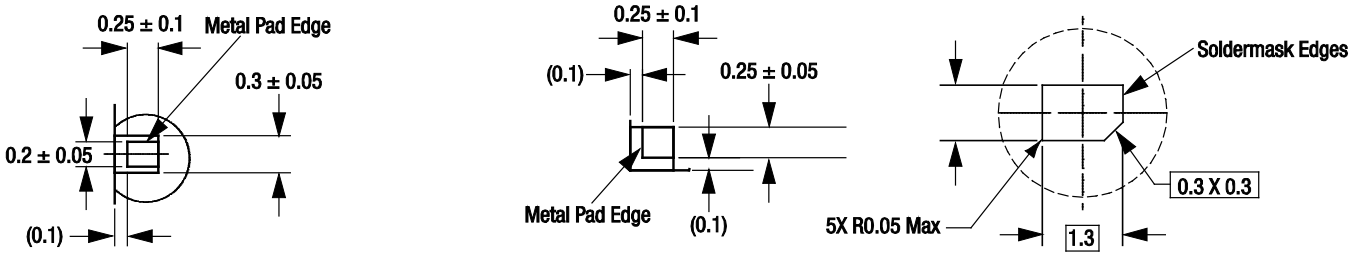
Figure 8. Typical Part Markings
(Top View)





All measurements are in millimeters

Dimensioning and tolerancing according to ASME Y14.5M-1994

S3324

Figure 9. SKY13484 22-Pin MCM Package Dimensions

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Figure 10. SKY13484 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13484 0.4-2.7 GHz SP5T + SP7T Receive Diversity Switch with MIPI RFFE Interface	SKY13484	SKY13484-EVB